FIBERBLAZE
A Silicom Company

fbC2CGg3 Supporting the fbCAPTURE framework

The Fiberblaze fb2CGg3 offers 2 x 100GE network connectivity and high speed capture to host memory with zero packet loss and packet processing.

The fbC2CG card is based on cutting edge Xilinx FPGA technology, providing packet filtering, advanced processing, traffic management, load balancing and host offloading mechanisms.

This high performance hardware platform connects to 100GE using QSFP28 modules, and performs packet processing, while delivering a sustained throughput to host memory of up to 224 Gbps.

The card use a single-slot PCIe solution through a 16-lane PCIe slot. It alos features a second PCIe connector for cable connection to a second PCIe slot. The second PCIe connector can also serve as a card-to-card interconnect path. Offering a combined solution for 4x100Gbps connections using combined features for effective traffic management and load balancing in NUMA environments.

The fbC2CGg3 is part of the fbCAPTURE family which provides a powerful and flexible Software API, as well as standard libpcap integration. Through the integration of fbCAPTURE API, applications gain support for all fbCAPTURE cards, covering Ethernet speeds from 1GE to 100GE.

NETWORK INTERFACE
- IEEE standard: IEEE 802.3 10 Gbit/s Ethernet
- Physical interface: 2 x QSFP28 port.
- Supported QSFP28 modules (CAUI-4)
  - 100GBASE-SR4 (850 nm)
  - 100GBASE-LR4 (1310 nm)
  - Planned PSM4, CLR4, CWDM4, ER4
  - 4x25GE Break-out modules
- Data rate: 2 x 100 Gbit/s
- Ethernet PHY directly embedded in FPGA for full packet control

HOST INTERFACE
- Physical bus connector: 16-lane PCIe
- PCIe bus type: 16 lane PCIe Gen1/Gen2/Gen3
- Optional 2nd PCIe cable connect
  - 16 lanes via host bifurcation
- PCIe compliant
- 64 logical channels that can be connected to DMA or egressed to physical output ports

ON BOARD MEMORY
- On board buffering for application robustness
- 16 GB 64 bit DDR4

PERFORMANCE
- Capture rate: full line rate, all interfaces
- Capture rate (bursts): full line rate, all interfaces
- Capture rate (sustained): full line rate, all interfaces
- Transmission rate (inline bypass): full line rate, all interfaces
- Transmission rate (daisy chain): full line rate, all interfaces

LATENCY
- Less than 3 µs to host memory
- Less than 3 µs from host memory to Tx
- Non-blocking sending, allowing user applications to operate independently

TIME STAMPING & SYNC
- Resolution = 3.2 ns
- Accuracy down to 20 ns
- Daisy chain PPS between multiple cards
- Optional external synchronization: PPS
- Optional PTP IEEE 1588-2008 sync card with RJ45 interface

CONFIGURATION
- Dual boot images with automatic fallback to fail-safe image
- Full firmware upgrades via supplied tools or fbCAPTURE API

ENVIRONMENT
- Physical dimensions: 3/4 length, standard height
- PCIe: 111 x 254 mm
- Weight: 238g
- Operational power consumption: Less than 39W
- Operating temperature: 0 – 55°C, 30 – 130°F
- Operating humidity: 20 – 80%
- Hardware compliance: RoHS, CE
- Passive cooling, with adequate host cooling
- Active cooling solution available

ADDITIONAL BOARD SUPPORT
- fbCAPTURE API
- On-board temperature sensor
- Multi-color status LEDs
- Link and Activity LEDs for each port

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The fbCAPTURE framework

The fbCAPTURE framework is a combination of FPGA firmware and a software API in C that utilises the full potential present in a range of FPGA based network interface cards from Fiberblaze. The fbCAPTURE Cards are designed with a combination of a powerful FPGA and large amounts of high speed onboard memory to ensure zero packet loss even at line rate performance. The fbCapture API is common for all the capture cards for 1GE, 10GE, 40GE and 100GE line rates. This simplifies system integration greatly, as support for multiple network rates can be achieved with the same integration efforts.

SOFTWARE API
- Same API for all Fiberblaze capture cards
- WinPCAP and LibPCAP compatibility
- C based API (DLL/Shared library)
- Linux, Windows & FreeBSD (on request)
- Multi Direct Memory Access streaming
- using up to 64 channels to host controlled memory buffer
- User error handlers
- No additional SW library dependencies

SERVER LOAD BALANCING
- Host server traffic load balancing supported
- Up to 64 channels to multiple host processes' memory
- Load balancing to external hosts via optical Tx interfaces
- Dual level load balancing. Hosts & CPUs
- Copy same PDU to multiple channels
- Distribution without CPU overhead using 2,3,5 and N tuple hashing or filter rules

SUPPORTED HARDWARE
- Fiberblaze cards for 1, 10, 40 and 100 Gbit/s using pluggable transceiver modules (SFP, SFP+, QSFP, CFP2, CFP4)
- Ethernet PHY embedded in FPGA for full packet control
- PCIe Gen1, Gen2 and Gen3 support for optimal host throughput
- Monitoring via SPAN port/optical splitters Ethernet auto-negotiation
- Limitless Daisy Chaining of monitored
- optical fibers between cards, at full signal strength, reducing number tapping of points

FILTERS
- A wide range of inline filters can be defined and combined in real-time to meet a variety of filtering requirements on a wide range of protocol header parameters

FILTERS (continued)
- Filter types available include ranges, pattern match, fixed/dynamic offset and value, bit masks and value, true/false, not, hash values, compounds and more on e.g.:
- Link layer:
  ARP, Tunnels (L2TP), MAC, VLAN incl. Stacked VLAN, MPLS, etc.
- Internet layer:
  IPv4, Ipv6, ICMP, RIP, OSPF, ECN, etc.
- Transport layer:
  UDP, TCP, SCTP, etc.
- Application layer:
  HTTP, FTP, LDAP, POP, RTP, SIP, SMTP, Telnet, GTPv1, GTPv2, RNSAP and RANAP via SIGTRAN, GTP-U payload headers etc.
- Option to allow on-wire error packets through

PACKET SLICING
- A wide range of slicing rules can be applied to conserve memory and storage by truncating packets
- Fixed length slicing
- Dynamic slicing where truncation may start from any specified header and include user definable number of bytes thereafter

PACKET DESCRIPTOR
- Captured packets can be enriched with descriptors generated by the adapter at line rate.
- PCAP Descriptor
- Standard Descriptor
- Multiple Descriptors
- Multiple time formats supported

PACKET PROCESSING
- Host acceleration of protocol parsing
- Zero copy PDU handling
- No protocol parsing needed for access to individual layers

PACKET DESCRIPTOR (continued)
- Packet layers indexing of protocol layers
- Optional insertion of alignment ticks (packets) in host memory buffer every 100ms

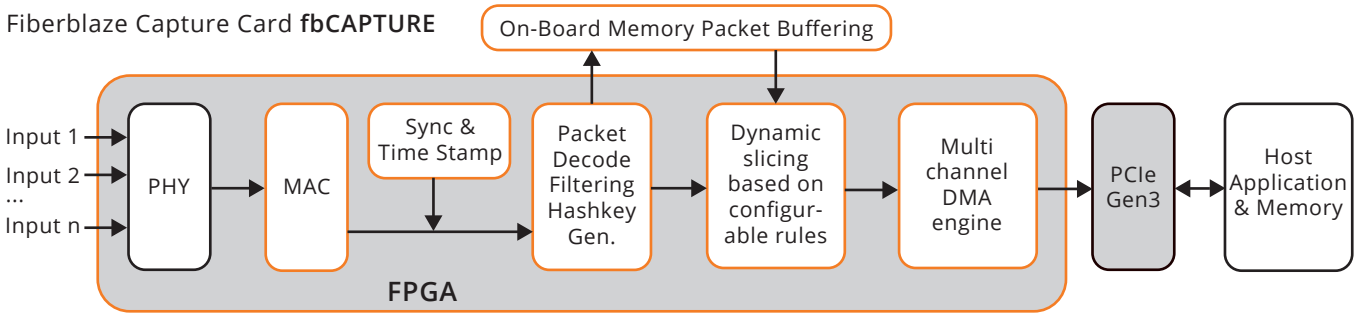
DEDUPLICATION
- Removal of duplicated packets
- Configurable duplication detection parameters

IP DEFRAGMENTATION
- IP fragments are correlated on-the-fly and processed as the initial fragment of the original packet
- Correlated fragment handling ensures that all related fragments are delivered to same channel as specified for the complete original packet
- True representation of on-wire packets

NETWORK STATISTICS
- Elaborated subset of RFC2819 RMON1
- Statistics each second for each interface
- Counters for special purpose firmwares
- Network counters include: Number of octets, CRC align errors, undersize packets, oversize packets incl Jumbo frames, packet size distribution & more
- Provided via API or via supplied independent Fiberblaze application

ON-BOARD SENSOR READINGS
- Temperature with preset minimum, maximum card operating temperature
- Optical signal level readings
- Link status
- Provided via API or via supplied independent Fiberblaze application

Fiberblaze Capture Card **fbCAPTURE**



Data rates: 1, 10, 40 100Gb/s